10. Fundamentals of RF Design and Fabrication Processes of Fan-Out Wafer/Level and Advanced RF Packages

Course Leaders: Ivan Ndip – Fraunhofer IZM/Brandenburg University of Technology and Markus Wöhrmann – Fraunhofer IZM

Course Description:
Due to their myriad of advantages in system-integration, fan-out wafer/panel-level packages (FO WLPs/PLPs) and other advanced RF packages (e.g., glass interposers and chip-embedding packages) will play a key role in the development of emerging electronic systems. The fabrication processes and RF performance of these packages will contribute significantly to the cost and performance of the entire system. The objective of this course is to provide and illustrate the fundamentals of the fabrication processes and RF design of these advanced packages for emerging RF/wireless applications.

An overview of distinct types of wafer-level packages, fan-out technologies, glass interposers and chip-embedding packages will first be given. This will be followed by a presentation of new fan-out-packaging and interposer-based concepts for emerging and future applications (e.g., 5G mmWave, mmWave radar sensors, 6G) as well as a thorough discussion of the materials and fabrication processes of FO-WLPs/PLPs, multilayered RDLs, glass interposers and chip embedding packages. The basics of efficient RF design and measurement of the fundamental building blocks of these advanced packages will be given for frequencies up to the millimeter-wave range. Finally, examples of these advanced packages designed and fabricated at Fraunhofer IZM will be discussed.

Course Outline:
1. Overview: Different Types of Wafer-Level Packages, Fan-Out Technologies, and Advanced RF Packages
2. Requirements of 5G Packaging and New Fan-Out Packaging Concepts for 5G mmWave Applications
3. Materials and Fabrication Processes: FO-WLPs/PLPs, Multi-Layered RDLs, Glass Interposers and Chip Embedding Packages
4. Fundamentals of RF Design and Measurement: FO-WLPs/PLPs, Glass Interposers and Chip-Embedding Packages
5. Examples of Advanced Packages Designed and Fabricated at Fraunhofer IZM

Who Should Attend:
Engineers, scientists, researchers, designers, managers, and graduate students interested in the fundamentals of electronic packaging as well as those involved in the process of electrical design, layout, processing, fabrication and/or system-integration of electronic packages for emerging applications (e.g., 5G, 6G, mmwave radar sensors) should attend.

Bio 1: Ivan Ndip is a full Professor at the Brandenburg University of Technology (BTU) in Germany. He has also been with Fraunhofer IZM for over 20 years, where he currently leads the Department of RF & Smart Sensor Systems. Prior to joining BTU, Ivan taught Graduate Courses in the Faculty of Electrical Engineering and Computer Sciences at the Technische Univerisität Berlin for 10 years. He has been teaching Professional Development Courses (PDCs) to practicing engineers and scientist worldwide for over 12 years. He has authored and co-authored over 230 scientific publications in peer-reviewed journals and conference proceedings, and has received numerous best paper awards as well as national and international awards. He holds over 35 German, European and US patents.

Ivan received the Dipl.-Ing. (M.Sc.) and Dr.-Ing. (Ph.D.) degrees in electrical engineering from the Technische Universität Berlin, and the Dr.-Ing. habil. degree also in electrical engineering from the Brandenburg University of Technology, Germany. He served as Director in the IMAPS Executive Board from 2016 to 2020. He is a Life Member and Fellow of IMAPS as well as Senior Member of IEEE.

Bio 2: Markus Wöhrmann (born 1984) received the M.Sc. electrical engineering at Technical University of Berlin in 2010. Since 2010 he is working on electrical and mechanical property estimation of thin film layers at the Technical University of Berlin. In 2016 he joined the Fraunhofer Institute for Reliability and Microintegration (IZM). He is leading the group “Lithography and Thin Film Polymers for Wafer-Level-Packaging” at the Fraunhofer IZM since 2019, where he is responsible for process development of RDL processing for Fan-In and Fan-Out Wafer Level Packaging.